REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed December 13, 2005.

Currently, claims 1, 3-12, 24-35 and 40-47 are pending.

I. Objections

The Examiner objected to claims 5 and 34 due to informalities. Applicant has amended claims 5 and 34 accordingly.

II. Drawings

The Examiner objected to the drawings and required that a legend such as "Prior Art" be added to Figures 1-3. Applicants have submitted a replacement page, as described above.

III. Allowed Claims

The Examiner has indicated that claims 25 and 33 contain allowable subject matter.

IV. Claim Rejections Under 35 U.S.C. §103

The Examiner rejected claims 1, 3-6, 8, 11, 12, 24, 26-29 and 31 as being obvious in light of Wong et al. (U.S. Patent 5,969,986) and Holzmann et al. (U.S. Patent 6,301,161). Because the cited prior art, alone or in combination, does not teach or suggest all of the limitations of Applicant's claims, Applicant asserts that claims 1, 3-6, 8, 11, 12, 24, 26-29 and 31 are in condition for allowance.

Claim 1 recites that "said one or more verification selection circuits cause a first subset of said non-volatile storage elements connected to said common control line to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements connected to said common control line are subjected to fine verification" with the "common control line connected to said non-volatile storage elements and in communication with said programming circuit ..." These limitations are not taught or suggested by the cited prior art.

Wong et al. discloses a memory system that includes "multiple memory arrays 130-1 to 130-N of non-volatile memory cells in respective read/write pipelines 110-1 to 110-N." [Wong

et al., col. 3, lines 44-48]. However, the Examiner admits at page 4 of the Office Action that Wong et al. does not disclose coarse and fine verification. Therefore, Wong et al. does not teach or suggest "said one or more verification selection circuits cause a first subset of said non-volatile storage elements connected to said common control line to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements connected to said common control line are subjected to fine verification..."

Holzmann et al. discloses coarse/fine programming. For example, Holzmann et al. states:

> The program pulse is divided into a series of coarse pulses and a series of fine pulses to store an analog signal in the non-volatile memory cell. After each programming pulse, the content of the cell is read using a read cycle and compared with the analog signal to be stored. The coarse pulses terminate when the desired coarse programmed level is approached and the programming is then switched to the fine stage where fine pulses are provided. The fine pulses terminate when the desired programmed level is reached. [Holzmann et al., col. 3, lines 19-27].

While Holzmann et al. does disclose coarse/fine programming, Holzmann et al. does not disclose the concurrent coarse/fine verification recited in claim 1 as "said one or more verification selection circuits cause a first subset of said non-volatile storage elements connected to said common control line to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements connected to said common control line are subjected to fine verification..."

Combining the prior art references, as proposed by the Examiner, also does not teach all of the limitations of Applicant's claims. The Examiner asserts that one of the memory arrays of Wong et al. can be performing coarse verification while another memory array can be performing fine verification. However, this scenario does not meet all of the limitations of claim 1, which requires that some of the non-volatile storage elements connected to the common control line are performing coarse verification while other non-volatile storage elements connected to the common control line are performing fine verification. On the other hand, the Examiner's proposed combination includes the storage elements in the coarse verification in one of the memory array and the storage elements in the fine verification in a different memory array. Because the storage elements are in different memory arrays, they are not connected to a

common control line. Figure 1 of Wong et al. does show the signals Vpp and Vvfy connected to each of the pipelines 110; however, these signals are not connected to the storage elements inside the memory arrays. Wong et al. even states that "Memory arrays 130 are separate in that erase, write, and read operations in one array 130 do not affect erase, write, and read operations in other arrays." [Wong et al., col. 4, lines 13-15]. As such, the proposed combination fails to teach or suggest all of the limitations of claim 1.

Applicant also notes that the Examiner has indicated that claim 25 is allowable, and claim 25 recites a common word line, which is one example of a common control line.

For all of the reasons discussed above, Applicant asserts that claim 1 is in condition for allowance. For the same reasons as discussed above with respect to claim 1, Applicant asserts that claims 3-12 are also in condition for allowance.

Claim 24 recites "providing a common programming signal to said non-volatile storage elements ... performing coarse verification for said one or more of said non-volatile storage elements that are in said coarse programming phase while concurrently performing fine verification for said one or more of said non-volatile storage elements that are in said fine programming phase." Thus, claim 24 requires that some of the non-volatile storage elements that receive the common programming signal perform coarse verification while some of the non-volatile storage elements that receive the common programming signal perform fine verification. As discussed above with respect to claim 1, these limitations are not taught by the proposed combination of prior art. Rather, the combination of prior art proposed by the Examiner contemplates one memory array performing coarse verification while another memory array is performing fine verification. The non-volatile storage elements in the different memory arrays do not receive a common programming signal. Therefore, the proposed combination fails to teach or suggest all of the limitations of claim 24.

For all of the reasons discussed above, Applicant asserts that claim 24 is in condition for allowance. For the same reasons as discussed above with respect to claim 24, Applicant asserts that claims 24-35 are also in condition for allowance.

The Examiner rejected claims 7, 9, 10, 30, 32, 34 and 35 as being obvious in light of Wong et al., Holzmann et al., and Guterman (U.S. Patent 6,222,762). Because the Examiner's rejection was based on the rejection of the independent claims (1 and 24) and the rejection of the

independent claims has been overcome as described above, Applicant asserts that claims 7, 9, 10, 30, 32, 34 and 35 are in condition for allowance for at least the same reasons as discussed above with respect to the independent claims..

V. New Claims

Applicant has added new claims 40-47. Claims 40-42 depend from claim 24 and, therefore, are patentable over the cited prior art for at least the same reasons as claim 24. Claim 43 depends from claim 1 and, therefore, is patentable over the cited prior art for at least the same reasons as claim 1.

Claim 44 recites "a common program signal" and "said one or more verification selection circuits cause a first subset of said non-volatile storage elements to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements are subjected to fine verification." Therefore, claim 44 is patentable over the cited prior art for at least the same reasons as claim 24.

Claim 45 recites "said programming circuit programs said non-volatile storage elements together as part of a common coarse/fine programming process; and ... said one or more verification selection circuits cause a first subset of said non-volatile storage elements to be subjected to coarse verification concurrently while a second subset of said non-volatile storage elements are subjected to fine verification." As discussed above, the combination of prior art proposed by the Examiner includes separate programming processes for each memory array, rather than a "common coarse/fine programming process" as recited in claim 45. Therefore, claim 45 is patentable over the cited prior art.

Claim 46 recites "said one or more verification selection circuits cause a first subset of said array of non-volatile storage elements to be subjected to coarse verification concurrently while a second subset of said array of non-volatile storage elements are subjected to fine verification." Thus, claim 45 recites that concurrent coarse and fine verification is performed in one memory array, while the proposed combination of prior art performs the coarse and fine verification in different memory arrays.

Claim 47 recites "providing a programming signal to a set of non-volatile storage elements being programmed together as part of a common coarse/fine programming process ...

performing coarse verification for said one or more of said non-volatile storage elements that are in said coarse programming phase while concurrently performing fine verification for said one or more of said non-volatile storage elements that are in said fine programming phase." Thus, claim 47 is patentable over the cited prior art for at least the same reasons as claim 45.

VI. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1, 3-12, 24-35 and 40-47 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document, including any fee for extension of time, which may be requested.

Respectfully submitted,

Date: March 3, 2006 By: Burt Magen

Burt Magen
Reg. No. 37,175

VIERRA MAGEN MARCUS & DENIRO LLP
575 Market Street, Suite 2500
San Francisco, California 94105
Telephone: 415.369.9660
Facsimile: 415.369.9665

AMENDMENTS TO THE DRAWINGS

The attached sheet of replacement drawings includes changes to Figures 1-3. This sheet, which includes Figures 1-3, replaces the original sheet including Figures 1-3. Figures 1-3 are amended by adding the legend "Prior Art."